10.6 A 90GHz 65nm CMOS Injection-Locked Frequency Divider

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Distance-control systems in automobiles increase the security and the driving comfort of the occupants. The frequency bands around 24 and 79GHz are intended for short range radar-based purposes while long-range radar solutions are allocated around 77GHz. Figure 10.6.1 shows the block diagram of a phase-locked loop (PLL) for such systems containing two cascaded divide-by-2 circuits (leading to a divide-by-4 configuration). In this paper, an injection-locked divider (ILD) is presented which is able to divide an input signal from 82 to 94.1GHz by two. Moreover, a divide-by-4 ILD is also reported with a locking range from 79.7 to 81.6GHz.

The schematic of the first divide-by-2 ILD (ILD1) is shown in Fig. 10.6.2. The divider core draws 7mA from a 0.56V supply and is designed and fabricated in a 65nm CMOS technology [1]. For an input power of 0dBm the locking range is 13.75% around a centre frequency of 88.8GHz. In a second design, ILD1 is followed by another divide-by-2 ILD (ILD2), leading to a two-stage divide-by-4 ILD (ILD/4) configuration (Fig. 10.6.1) with a center frequency of 80.8GHz. For ILD/4 a locking range of 2.35% is measured for an input signal power of –1dBm.

In a PLL, the first divider behind the VCO is the most critical one because its input frequency is the highest. Static and regenerative dividers offer higher bandwidths but their maximum achievable frequency of operation is limited by the intrinsic capacitances. In automotive radar systems with a fundamental VCO frequency of 77GHz an LC-ILD is the concept of choice because the parasitic capacitances are used as part of the LC resonance tank. Distance-control systems based on frequency-modulated continuous-wave (FMCW), as considered here, are using linear frequency ramps for optimum obstacle detection. The measurement precision is directly related to the linearity of the frequency ramp. Therefore, it is necessary for the dividers in the PLL to be able to continuously divide the VCO signal without any adjustments during the measurement process. Recently published divider architectures use division ratios of three [2] and four [3] to save additional circuitry. The locking ranges (LRs) of these structures are much smaller compared to divide-by-2 ILDs because of the degradation of locking efficiency for harmonics higher than two. In order to enhance the LR, varactors have to be adjusted to shift the resonance frequency of these structures. Therefore, in this work ILD1 and ILD2 are developed which divide the input signal within the whole LR without any external control.

The basic topology of the presented ILD1 (Fig. 10.6.2) is proposed in [4]. It consists of an NMOS negative-impedance converter (NIC) to compensate for tank losses, a center-tapped inductor to resonate with the tank capacitances and a PMOS and an NMOS transistor for direct injection locking. Using two complementary transistor types makes an excitation with a differential input signal possible. Thus, the divider provides a symmetrical load for a driving VCO. The input pads are connected with the locking transistors via microstrip lines. By varying the dc operating point of the locking transistors, the locking range can be enhanced [5]. The divider is buffered by a cascode to drive the output load.

Particular attention is paid to the sizing of the divider core elements. The channel widths of the locking transistors M1 and M2 are increased to boost the locking efficiency and hence the locking range. The upper bound of this approach is set by the VCO that has to drive the capacitive load of M1 and M2 at twice the resonance frequency of the divider. In order to further increase the locking range, the tank quality factor Q_{tank} is reduced by adding a lossy varactor to the core. The lower bound of Q_{tank} depends on the transconductance of the NIC. If Q_{tank} is reduced too much, the oscillation dies away. The varactor is also used as a coarse tuning element to adjust the center frequency f_0. For a given capacitance of the load and the locking transistors, the inductance value is traded off with the capacitances of the NIC and the varactor. However, increasing the width of the locking transistors results in a higher tank capacitance of the divider. Furthermore, reducing Q_{tank} requires a larger transconductance of the NIC that also results in a higher tank capacitances. Therefore, high frequency has to be traded off with wide locking range.

A micrograph of the chip is shown in Fig. 10.6.3. The measured locking ranges of the presented ILD1 are shown in Fig. 10.6.4. Depending on the DC voltage $V_{dc1,n}$ applied to the NMOS locking transistor, the center frequency is shifted between 88 and 89GHz. For a single-ended excitation at the input of the NMOS locking transistor, a maximum locking range of 12.1GHz is achieved for $V_{dc1,n}$ = 1.2 V. With an excitation at the input of the PMOS locking transistor, a maximum locking range of 2.8GHz is achieved for $V_{dc1,p}$ = 0 V. This shows that the NMOS transistor is more suitable for injection locking than the PMOS transistor. As $V_{dc1,n}$ directly affects Q_{tank} [5], the output power of the divider decreases with increasing $V_{dc1,n}$ (insert in Fig. 10.6.4).

As shown in Fig. 10.6.1, ILD/4 is realized in another design by cascading ILD2 and ILD1. In contrast to Fig. 10.6.2, in ILD2 the inductor is replaced by a coil without centre tapping and an additional PMOS NIC. The additional capacitances of the PMOS transistors in the tank of ILD2 are less critical since the resonance frequency is half of ILD1. Figure 10.6.5 shows the measured input sensitivity of ILD2. For $V_{dc2,n}$ = 1.2V, a maximum locking range of 8GHz and a self-resonance frequency f_0 of 19.3GHz are achieved in a stand-alone version of ILD2. Due to the large locking transistors of ILD2, f_0 of ILD1 is reduced to 41GHz in the cascade. For $V_{dc1,n}$ = 0V, the spectrum of the free running ILD/4 is shown in Fig. 10.6.6 together with an applied input signal of 80GHz. Increasing $V_{dc1,n}$ up to 1.2V leads to a maximum measured LR of 1.9GHz. With respect to the large locking ranges of the stand-alone versions of ILD1 and ILD2, this small value for ILD/4 has the following cause: The output of ILD1 is directly connected to the locking transistors of ILD2. Therefore, the DC voltage of the locking transistors $V_{dc2n,p}$ is only 0.56 V which results in a much smaller achievable locking range of ILD2. A comparison of the presented ILDs regarding locking range and power consumption to other recently published works is shown in Fig. 10.6.7.

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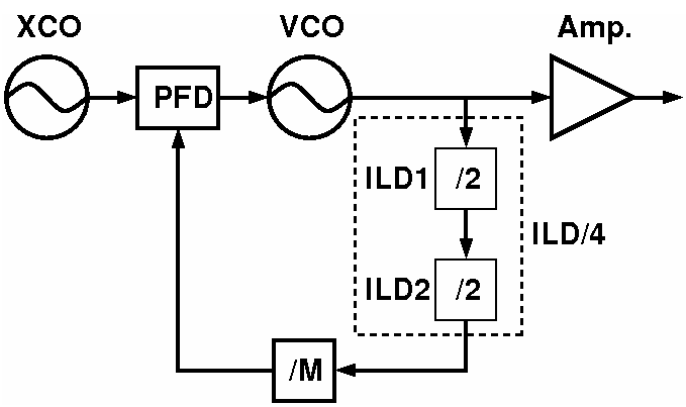

Figure 10.6.1: Block diagram of the PLL including ILDs.

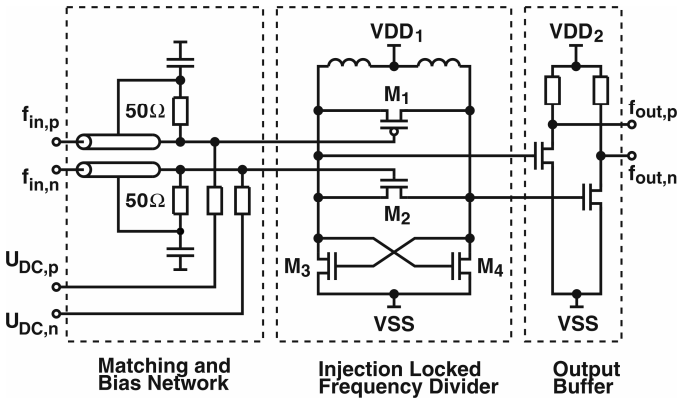

Figure 10.6.2: Schematic diagram of ILD1.

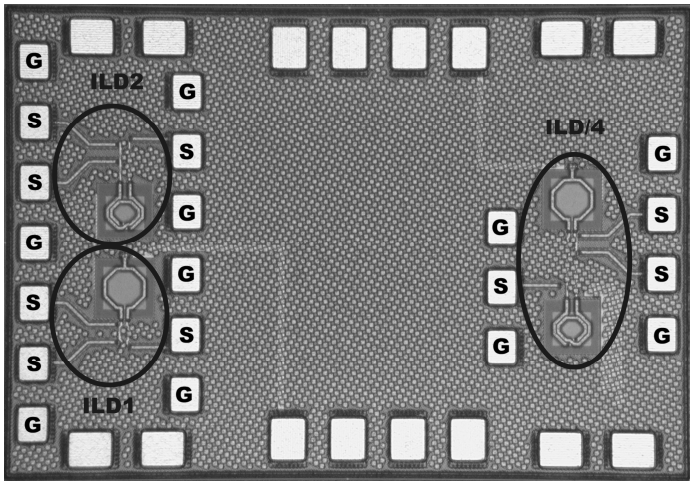

Figure 10.6.3: Chip micrograph of ILDs (1150×850μm²).

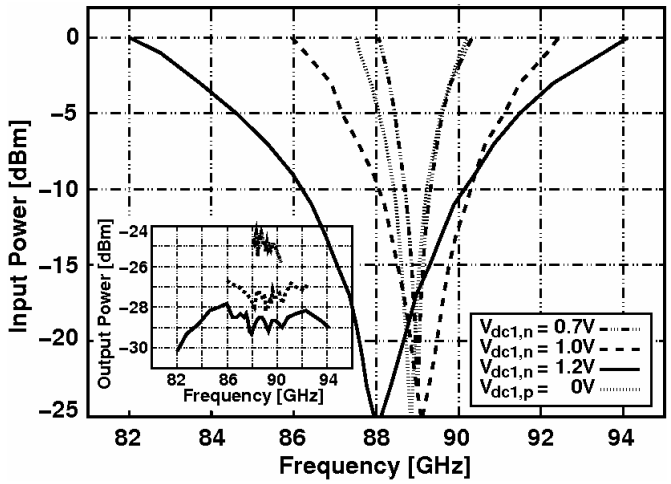

Figure 10.6.4: Measured input sensitivity curve of ILD1.

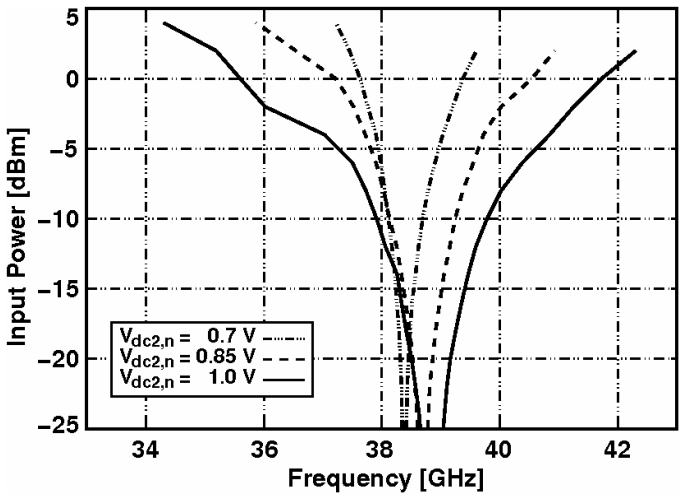

Figure 10.6.5: Measured input sensitivity curve of ILD2.

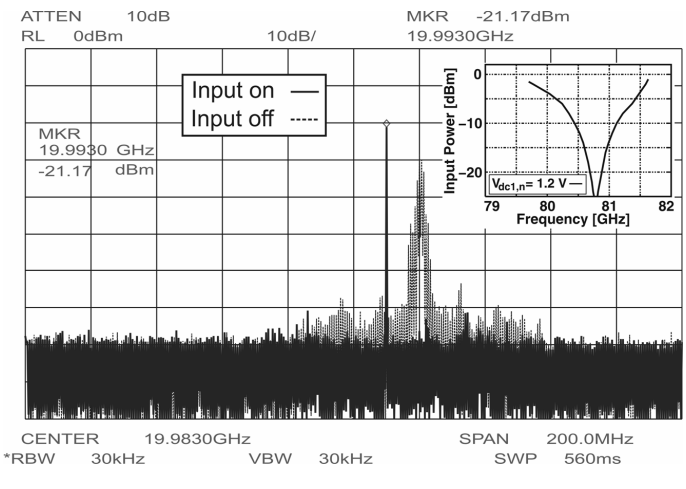

Figure 10.6.6: Measured output signal of ILD/4 for $U_{dc1,}$n = 0V.

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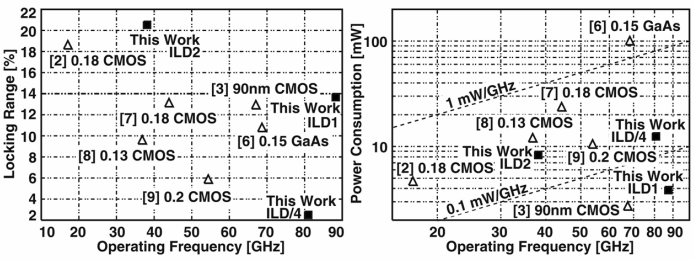

Figure 10.6.7: ILD Performance Comparison.

